What is claimed is:

- 1. A program development support apparatus
- 2 comprising:
- a CPU (Central Processing Unit) for executing
- 4 a target program and outputting instruction
- 5 address/instruction code data;
- 6 event management means for asserting and
- 7 outputting a section trace start signal upon detecting
- 8 that the instruction address/instruction code data from
- 9 said CPU matches one of a predetermined instruction
- 10 address and predetermined instruction code set as an
- 11 event condition in advance;
- 12 trace data generation means for, when an
- 13 instruction code of the instruction address/instruction
- 14 code data from said CPU is a branch instruction, or the
- 15 section trace start signal from said event management
- 16 means is active, outputting an uncompressed instruction
- 17 address as trace data, and when the instruction address
- 18 of the instruction address/instruction code data is not
- 19 the branch instruction, and the section trace start
- 20 signal is not active, generating a plurality of
- 21 compressed instruction addresses by compressing the
- 22 instruction address of the instruction
- 23 address/instruction code data, and then combining the
- 24 compressed instruction addresses and outputting the
- 25 compressed instruction addresses as the trace data; and

- a trace memory for storing the trace data from 27 said trace data generation means.
 - 2. An apparatus according to claim 1, wherein
 - 2 said event management means keeps a data latch
 - 3 signal active during a predetermined period and
 - 4 outputting the data latch signal, and
 - 5 said trace data generation means receives the
 - 6 instruction address/instruction code data from said CPU
 - 7 and the section trace start signal from said event
 - 8 management means and, when the data latch signal from
 - 9 said event management means is active, latches the
- 10 instruction address/instruction code data.
 - 3. An apparatus according to claim 2, wherein
 - 2 said event management means comprises
 - 3 event setting means in which event setting
 - 4 data containing the predetermined instruction
 - 5 address/instruction code as the event condition and the
 - 6 active period of the data latch signal are set in
 - 7 advance, and
 - 8 event detection means for, upon detecting that
- 9 the instruction address/instruction code contained in
- 10 the event setting data output from said event setting
- 11 means matches the instruction address/instruction code
- 12 of the instruction address/instruction code data from
- 13 said CPU, asserting and outputting the section trace

- 14 start signal and asserting the data latch signal during
- 15 the active period set in said event setting means and
- 16 outputting the data latch signal.
 - 4. An apparatus according to claim 2, wherein
- 2 said trace data generation means comprises
- 3 instruction address/instruction code latch
- 4 means for latching the instruction address/instruction
- 5 code data from said CPU during the active period of the
- 6 data latch signal and outputting the instruction
- 7 address/instruction code,
- 8 instruction address data compression means for,
- 9 when a received uncompressed data selection signal is
- 10 active, outputting the instruction address from said
- 11 instruction address/instruction code latch means as the
- 12 compressed instruction address, and when the
- 13 uncompressed data selection signal is not active,
- 14 outputting difference data obtained by subtracting an
- 15 immediately preceding instruction address from a current
- 16 instruction address as the compressed instruction
- 17 address,
- 18 branch instruction determination means for
- 19 determining whether the instruction code from said
- 20 instruction address/instruction code latch means is the
- 21 branch instruction, and upon determining that the
- 22 instruction code is the branch instruction, asserting
- 23 and outputting a branch instruction detection signal,

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24 trace control means for, when the received 25 uncompressed data selection signal is active, outputting 26 the compressed instruction address from said instruction 27 address data compression means as trace data, and when 28 the uncompressed data selection signal is not active, 29 combining a plurality of continuously received compressed instruction addresses in accordance with a 30 31 bit width of said trace memory and outputting the 32 combined instruction addresses as the trace data, and 33 outputting a trace data write signal for instructing 34 said trace memory to write the trace data and a trace 35 memory address for designating a storage address of said 36 trace memory, and 37 OR means for asserting and outputting the 38 uncompressed data selection signal when at least one of 39 the branch instruction detection signal from said branch instruction determination means and the section trace 40

5. An apparatus according to claim 4, wherein
2 said apparatus further comprises frame address
3 comparison means for asserting and outputting a frame
4 match signal when the instruction address/instruction
5 code contained in the event setting data output from
6 said event setting means matches the trace memory
7 address from said trace control means, and
8 said OR means asserts and outputs the

start signal from said event management means is active.

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- 9 uncompressed data selection signal when at least one of
- 10 the branch instruction detection signal from said branch
- 11 instruction determination means, the section trace start
- 12 signal from said event detection means, and the frame
- 13 match signal from said frame address comparison means is
- 14 active.
 - 6. A program development support apparatus
- 2 comprising:
- a trace memory for compressing and storing an
- 4 instruction address that has traced a program; and
- 5 event detection means for, upon detecting one
- 6 of a preset predetermined instruction address and
- 7 predetermined instruction code, controlling to write an
- 8 instruction address, in which one of the predetermined
- 9 instruction address and predetermined instruction code
- 10 is stored, in said trace memory as uncompressed data.